

## AS1710/AS1712

### High-Output-Drive, 10MHz, 10V/ $\mu$ s, Rail-to-Rail I/O Op Amps with Shutdown

#### 1 General Description

The AS1710/AS1712 are low-offset, high-output CMOS op-amps that deliver 200mA of peak output current from a single supply (2.7V to 5.5V).

These devices were specifically designed to drive typical headset levels ( $32\Omega$ ), as well as bias RF power amplifiers for wireless handset applications.

The devices are available as the standard products shown in Table 1. See also [Ordering Information on page 18](#).

Table 1. Standard Products

| Model   | Description                 | Package         |
|---------|-----------------------------|-----------------|
| AS1710A | Single Op Amp with Shutdown | SC70-6          |
| AS1710B | Single Op Amp               | SC70-5          |
| AS1712A | Quad Op Amp with Shutdown   | TQFN-16 (3x3mm) |

These rail-to-rail I/O, wide-bandwidth amplifiers exhibit a high slew rate of 10V/ $\mu$ s and a gain-bandwidth product of 10MHz.

The integrated shutdown feature (not included in B versions) drives the output low.

These devices operate over the entire industrial temperature range (-40°C to +85°C).

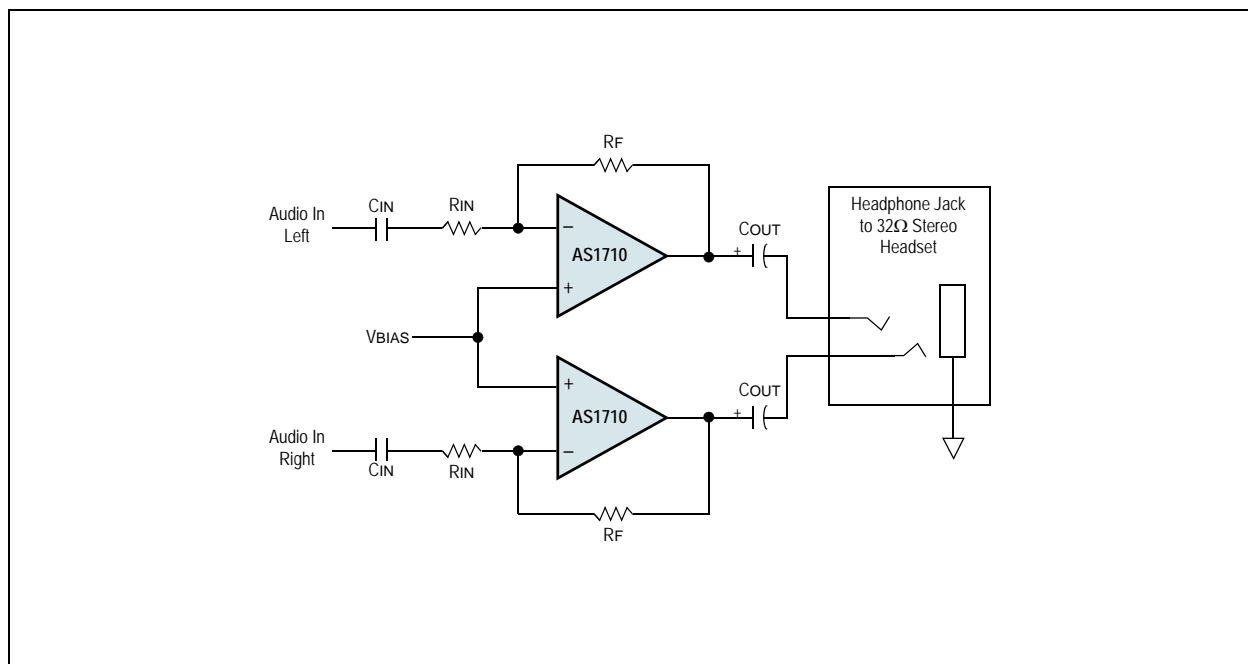
#### 2 Key Features

- Constant Output Drive Capability: 50mA
- Rail-to-Rail Input and Output
- Supply Current: 1.6mA
- Single-Supply Operation: 2.7V to 5.5V
- Gain-Bandwidth Product: 10MHz
- High Slew Rate: 10V/ $\mu$ s
- Voltage Gain: 100dB ( $R_{LOAD} = 100k\Omega$ )
- Power-Supply Rejection Ratio: -85dB
- No Phase Reversal for Overdriven Inputs
- Unity-Gain Stable for Capacitive Loads: Up to 100pF
- Shutdown Mode (AS1710A) Current: 1nA typ
- Package Types:
  - SC70-6
  - SC70-5
  - TQFN-16 (3x3mm)

#### 3 Applications

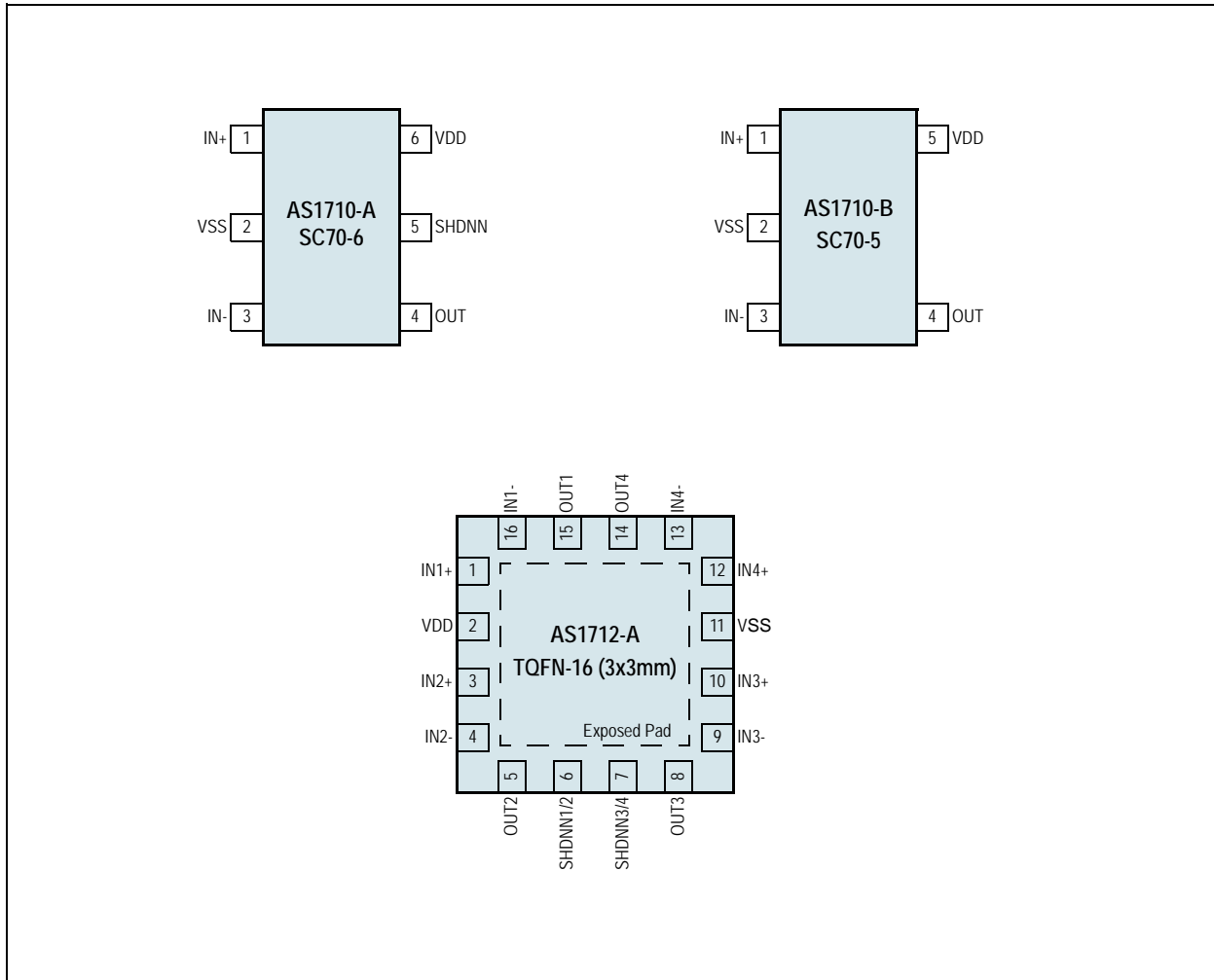
The devices are ideal for portable/battery-powered audio applications, portable headphone speaker drivers ( $32\Omega$ ), hands-free mobile phone kits, TFT panels, sound ports/cards, set-top boxes, biasing controls, DAC converter buffers, transformer/line drivers, motor drivers, and any other battery-operated audio device.

Figure 1. AS1710 - Typical Application



## 4 Pin Assignments

Figure 2. Pin Assignments (Top View)



### 4.1 Pin Descriptions

Table 2. Pin Descriptions

| Pin Number   | Pin Name    | Description   |
|--------------|-------------|---|
| See Figure 2 | IN+         | Non-inverting Input   |
|              | IN-         | Inverting Input   |
|              | VDD         | Positive Supply Input   |
|              | VSS         | Negative Supply Input. This pin must be connected to ground in single-supply applications.  |
|              | SHDNN       | Active Low Shutdown Control   |
|              | OUT         | Amplifier Output  |
|              | Exposed Pad | Exposed Pad. This pin also functions as a heat sink. Solder it to a large pad or to the circuit-board ground plane to maximize power dissipation. |

## 5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 3](#) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in [Electrical Characteristics on page 4](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

| Parameter  | Min                | Max          | Units | Comments |  |
|--|--------------------|--------------|-------|----------|--|
| <b>Electrical Parameters</b>                     |                    |              |       |          |  |
| Supply Voltage (VDD to VSS)                      |                    | +7           | V     |          |  |
| Supply Voltage (All Other Pins)                  | VSS<br>- 0.3       | VDD<br>+ 0.3 | V     |          |  |
| Output Short-Circuit Duration to VDD or VSS      |                    | 1            | s     |          |  |
| <b>Thermal Information</b>                       |                    |              |       |          |  |
| Continuous Power Dissipation                     | SC70-5             |              | 247   | mW       | Derate at 31mW/°C above 70°C   |
|  | SC70-6             |              | 245   |          |  |
| Thermal Resistance $\Theta_{JA}$                 | TQFN-16<br>(3x3mm) |              | 33    | °C/W     | on PCB   |
| <b>Temperature Ranges and Storage Conditions</b> |                    |              |       |          |  |
| Storage Temperature Range                        | -65                | +150         |       | °C       |  |
| Junction Temperature                             |                    | +150         |       | °C       |  |
| Package Body Temperature                         |                    | +260         |       | °C       | The reflow peak soldering temperature (body temperature) specified is in accordance with <i>IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices"</i> .<br>The lead finish for Pb-free leaded packages is matte tin (100% Sn). |
| Humidity non-condensing                          | 5                  | 85           |       | %        |  |
| Moisture Sensitive Level                         |                    | 1            |       |          | Represents a maximum floor life time of unlimited  |

## 6 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed by production tests or SQC (Statistical Quality Control) methods.

### 6.1 DC Electrical Characteristics

$V_{DD} = 2.7V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_{LOAD} = \text{Infinite}$ ,  $V_{SHDNN} = V_{DD}$ , Typical values at  $T_{AMB} = 25^{\circ}C$ .

Table 4. DC Electrical Characteristics

| Symbol     | Parameter                                       | Condition  | Min                                 | Typ               | Max               | Unit |    |
|------------|---|--|-------------------------------------|-------------------|-------------------|------|----|
| TAMB       | Operating Temperature Range                     |  | -40                                 |                   | +85               | °C   |    |
| VDD        | Supply Voltage Range                            | Inferred from Power Supply Rejection Ratio Test                    | 2.7                                 |                   | 5.5               | V    |    |
| VOFFSET    | Input Offset Voltage                            |  | -3                                  | 0.6               | +3                | mV   |    |
| IBIAS      | Input Bias Current                              | $V_{CM} = V_{SS}$ to $V_{DD}$                                      |                                     | 50 <sup>1</sup>   |                   | pA   |    |
| IOFFSET    | Input Offset Current                            | $V_{CM} = V_{SS}$ to $V_{DD}$                                      |                                     | 50 <sup>1</sup>   |                   | pA   |    |
| RIN        | Input Resistance                                |  |                                     | 1000 <sup>1</sup> |                   | MΩ   |    |
| VCM        | Common Mode Input Voltage Range                 | Inferred from Common Mode Rejection Ratio <sup>1</sup>             | VSS                                 |                   | VDD               | V    |    |
| CMRR       | Common Mode Rejection Ratio                     | $V_{SS} < V_{CM} < V_{DD}$   | -45                                 | -70               |                   | dB   |    |
| PSRR       | Power Supply Rejection Ratio                    | $V_{DD} = 2.7$ to $5.5V$   | -70                                 | -85               |                   | dB   |    |
| ROUT       | Shutdown Output Impedance                       | $V_{SHDNN} = 0V$ (A-Versions)                                      |                                     | 130 <sup>1</sup>  |                   | Ω    |    |
| VOUT-SHDNN | Shutdown Output Voltage                         | $V_{SHDNN} = 0V$ , $R_{LOAD} = 2k\Omega$ to $V_{DD}$ (A-Versions)  |                                     | 170               | 300               | mV   |    |
| AVOL       | Large Signal Voltage Gain                       | $V_{SS} + 0.20V < V_{OUT} < V_{DD} - 0.20V$                        | $R_{LOAD} = 100k\Omega$             | 85                | 100               |      | dB |
|            |   |  | $R_{LOAD} = 2k\Omega$               | 79                | 92                |      |    |
|            |   |  | $R_{LOAD} = 200\Omega$              | 69                | 80                |      |    |
| VOUT       | Output Voltage Swing                            | $V_{DD} - V_{OH}$ or $V_{OL} - V_{SS}$                             | $R_{LOAD} = 32\Omega$               |                   | 350               | 650  | mV |
|            |   |  | $R_{LOAD} = 200\Omega$              |                   | 70                | 120  |    |
|            |   |  | $R_{LOAD} = 2k\Omega$               |                   | 9                 | 20   |    |
|            | Output Voltage                                  | $V_{DD} - V_{OH}$ or $V_{OL} - V_{SS}$                             |                                     |                   |                   | mV   |    |
|            |   |  | $I_{LOAD} = 10mA$ , $V_{DD} = 2.7V$ | 55                | 100               |      |    |
|            |   |  | $I_{LOAD} = 30mA$ , $V_{DD} = 5V$   | 100               | 180               |      |    |
| IOUT       | Output Source/Sink Current                      | $V_{DD} = 2.7V$ ,<br>$V_{-} = V_{CM}$ , $V_{+} = V_{CM} \pm 100mV$ |                                     | 100               |                   | mA   |    |
|            |   | $V_{DD} = 5.0V$ ,<br>$V_{-} = V_{CM}$ , $V_{+} = V_{CM} \pm 100mV$ |                                     | 200               |                   |      |    |
| IDD        | Quiescent Supply Current per Op Amp Output      | $V_{DD} = 2.7V$ , $V_{CM} = V_{DD}/2$                              |                                     | 1.6               | 3.2               | mA   |    |
|            |   | $V_{DD} = 5.0V$ , $V_{CM} = V_{DD}/2$                              |                                     | 2.3               | 4.6               |      |    |
| IDD-SHDNN  | Shutdown Supply Current per Op Amp (A-Versions) | $V_{SHDNN} = 0V$   | $V_{DD} = 2.7V$                     | 1                 | 2000 <sup>1</sup> | nA   |    |
|            | SHDNN Logic Threshold (A-Versions)              | Shutdown Mode  |                                     |                   | $V_{SS} + 0.3$    | V    |    |
|            |   | Normal Operation   |                                     |                   | $V_{DD} - 0.3$    |      |    |
|            | SHDNN Input Bias Current                        | $V_{SS} < V_{SHDNN} < V_{DD}$ (A-Versions)                         |                                     |                   | 50 <sup>1</sup>   | pA   |    |

1. Guaranteed by design.

## 6.2 AC Electrical Characteristics

$V_{DD} = 2.7V$ ,  $V_{SS} = 0V$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} = V_{DD}/2$ ,  $R_{LOAD} = \text{Infinite}$ ,  $V_{SHDNN} = V_{DD}$ , Typical values at  $T_{AMB} = 25^{\circ}C$ .

Table 5. AC Electrical Characteristics

| Symbol  | Parameter                            | Conditions  | Min | Typ  | Max | Units           |
|---------|--------------------------------------|---|-----|------|-----|-----------------|
| GBWP    | Gain-Bandwidth Product               | $V_{CM} = V_{DD}/2$                                   |     | 10   |     | MHz             |
| FPBW    | Full-Power Bandwidth                 | $V_{OUT} = 2V_{P-P}$ , $V_{DD} = 5V$                  |     | 2.5  |     | MHz             |
| SR      | Slew Rate                            |   |     | 10   |     | V/ $\mu$ s      |
| PM      | Phase Margin                         |   |     | 70   |     | deg             |
| GM      | Gain Margin <sup>1</sup>             |   |     | 15   |     | dB              |
| THD+N   | Total Harmonic Distortion Plus Noise | $f = 10kHz$ , $V_{OUT} = 2V_{P-P}$ , $A_{VCL} = 1V/V$ |     | 0.05 |     | %               |
| CIN     | Input Capacitance                    |   |     | 6    |     | pF              |
| en      | Voltage-Noise Density <sup>1</sup>   | $f = 1kHz$  |     | 15   |     | nV/ $\sqrt{Hz}$ |
|         |                                      | $f = 10kHz$   |     | 10   |     |                 |
|         | Capacitive-Load Stability            | $A_{VCL} = 1V/V$ , no sustained oscillations          |     | 100  |     | pF              |
| tSHDN   | Shutdown Time (AS1710A)              |   |     | 1    |     | $\mu$ s         |
| tENABLE | Enable Time from Shutdown (AS1710A)  |   |     | 7    |     | $\mu$ s         |
| tON     | Power-Up Time                        |   |     | 20   |     | ns              |

1. Guaranteed by design.

## 7 Typical Operating Characteristics

$V_{DD} = 2.7V$ ;  $V_{SS} = 0V$ ;  $V_{CM} = V_{DD}/2$ ;  $V_{OUT} = V_{DD}/2$ ;  $R_{LOAD} = \infty$ ;  $V_{SHDN} = V_{DD}$   $T_{AMB} = +25^{\circ}C$  (unless otherwise specified).

Figure 3. Gain and Phase vs. Frequency

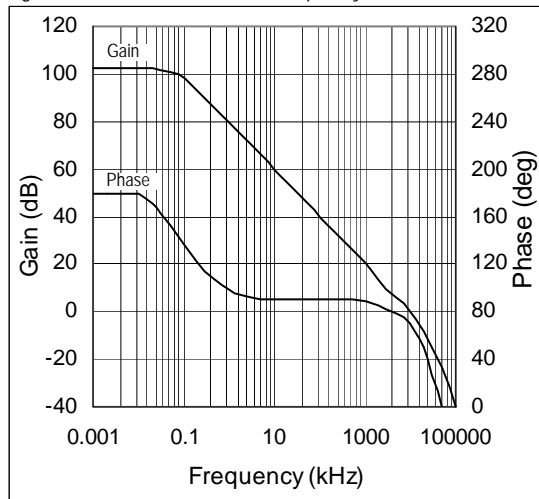


Figure 4. Gain and Phase vs. Frequency,  $C_{LOAD} = 100pF$

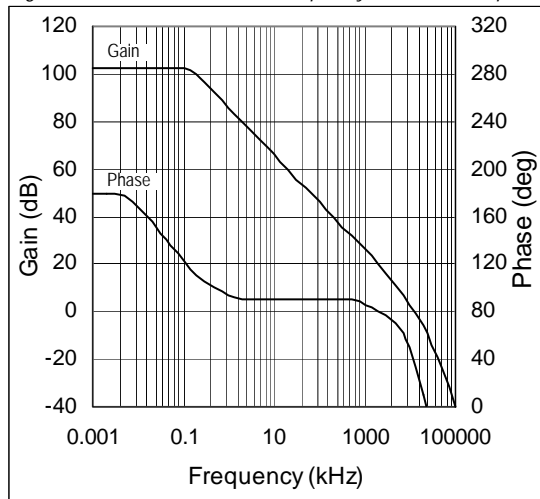


Figure 5. PSRR vs. Frequency

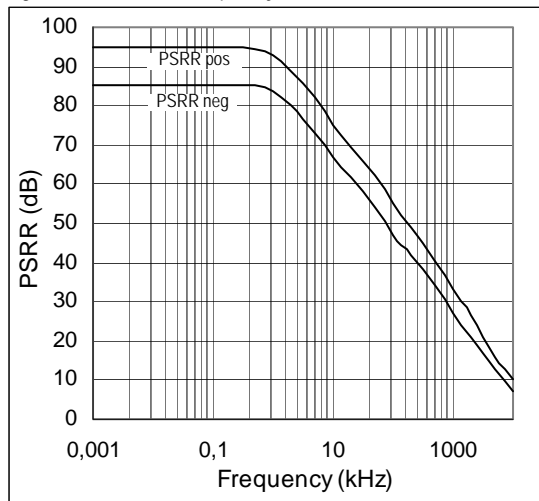


Figure 6. CMRR vs. Frequency

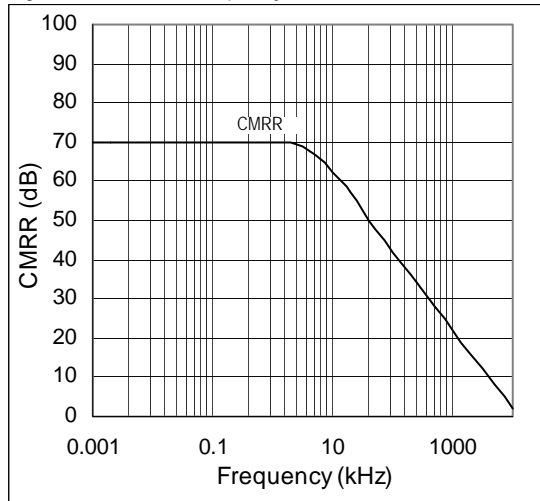


Figure 7. Supply Current vs. Temperature

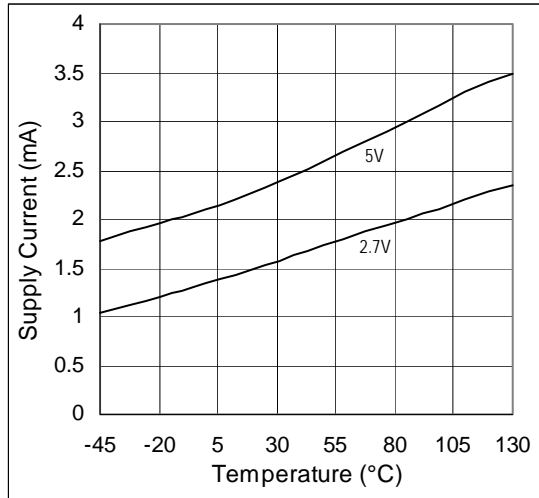


Figure 8. Shutdown Current vs. Temperature

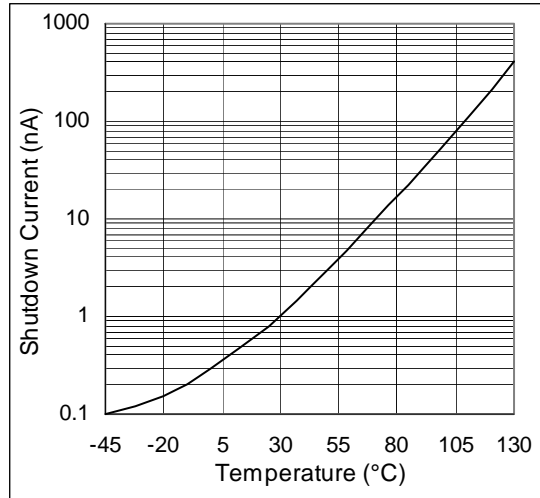


Figure 9. Supply Current vs. Common-Mode Voltage

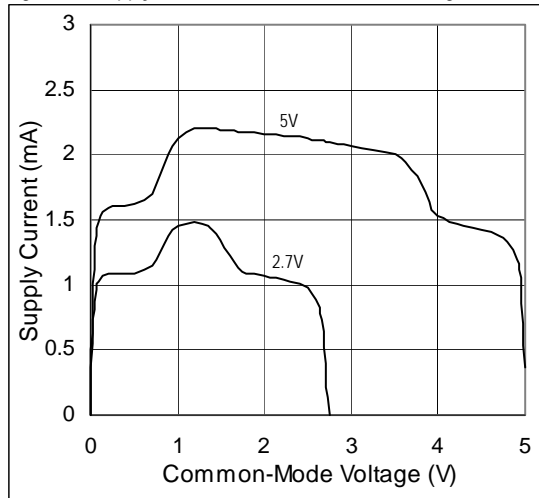


Figure 10. Input Voltage Noise vs. Frequency

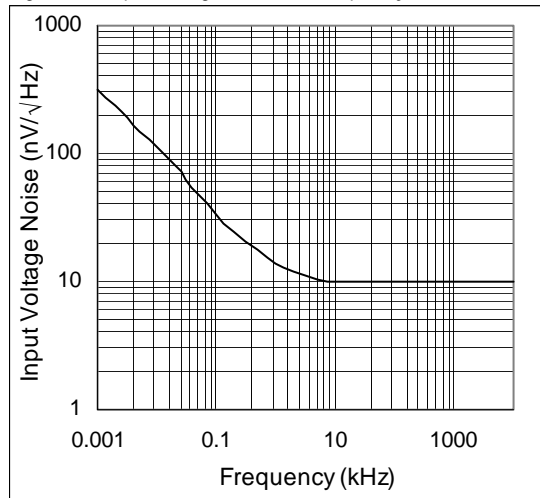


Figure 11. Output Voltage vs. Output Current, sourcing

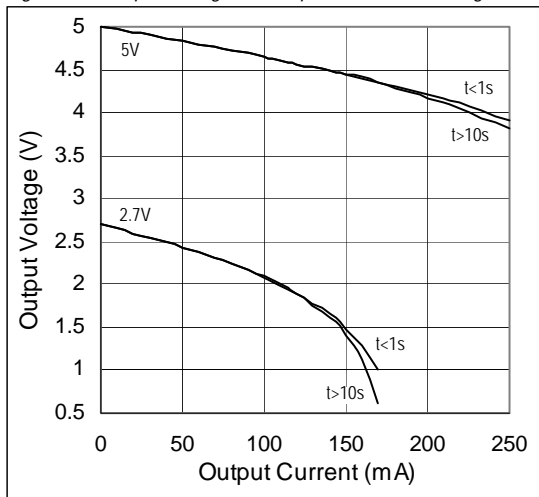


Figure 12. Output Voltage vs. Output Current, sinking

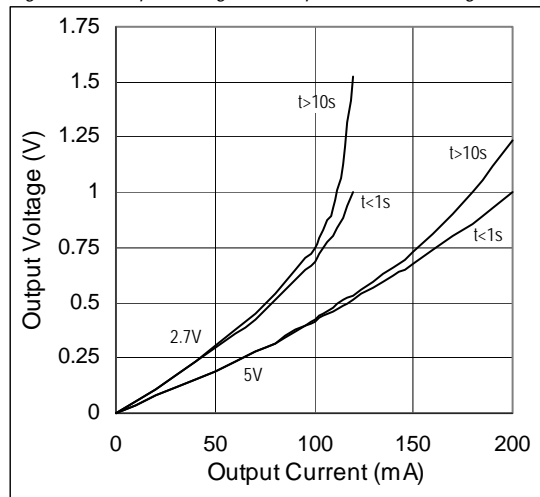


Figure 13. Output Swing High vs. Temperature

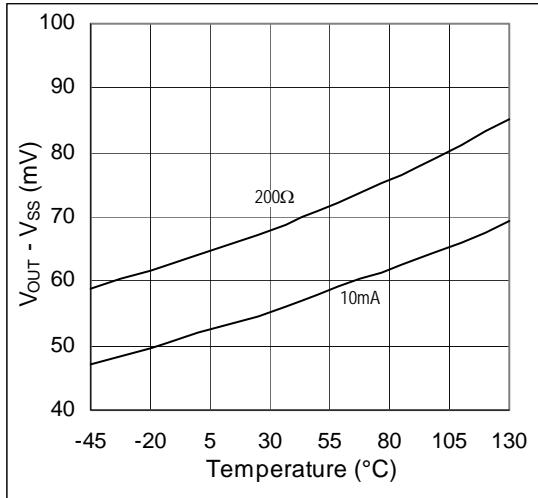


Figure 14. Output Swing Low vs. Temperature

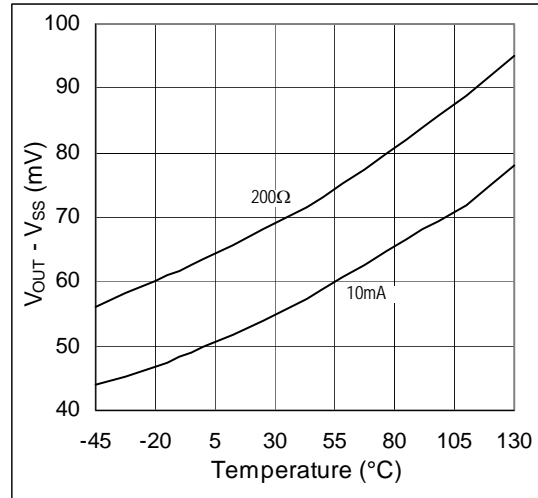


Figure 15. Transient Response, 100mV, 10pF load

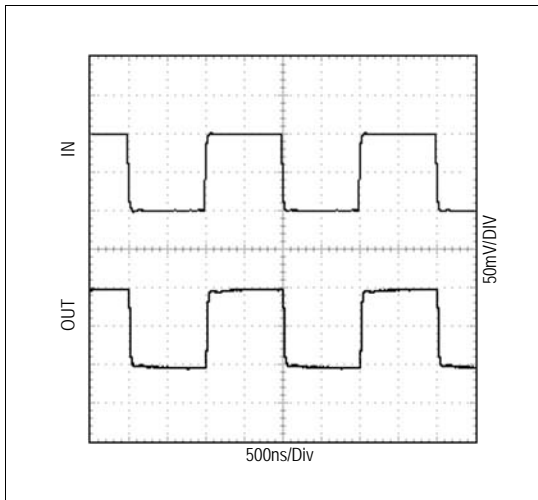


Figure 16. Transient Response, 100mV, 100pF load

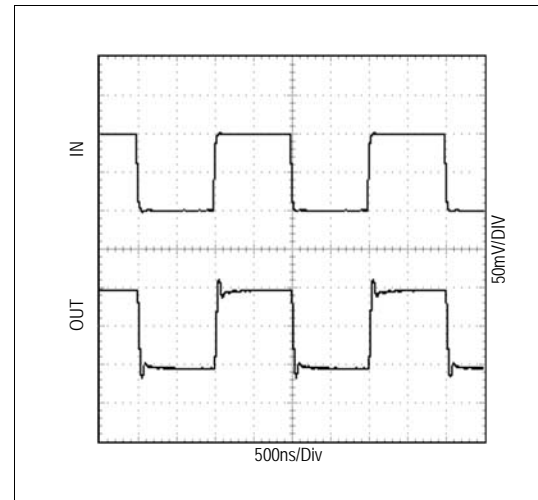


Figure 17. Transient Response, 1V, 10pF load

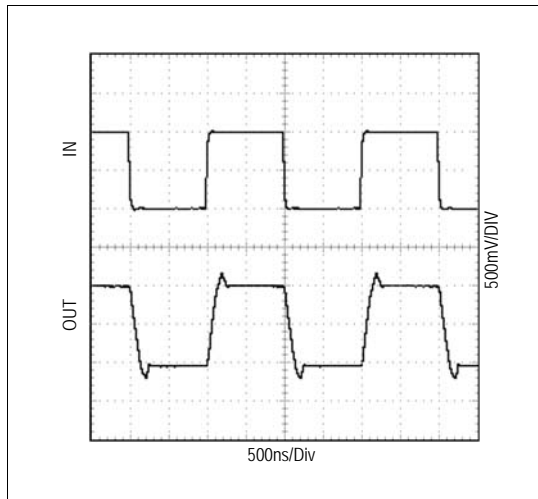


Figure 18. Transient Response, 1V, 100pF load

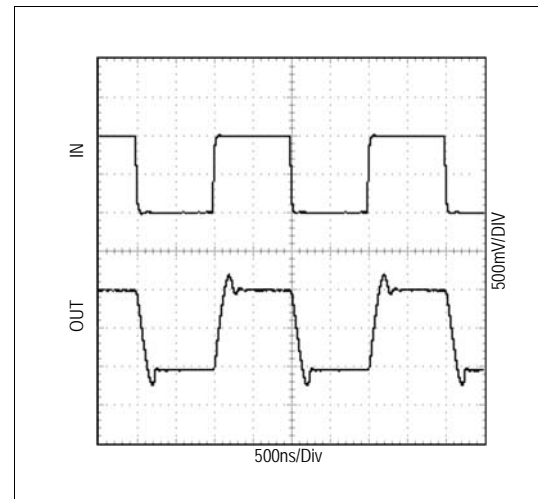


Figure 19. Transient Response, 2V, 10pF load

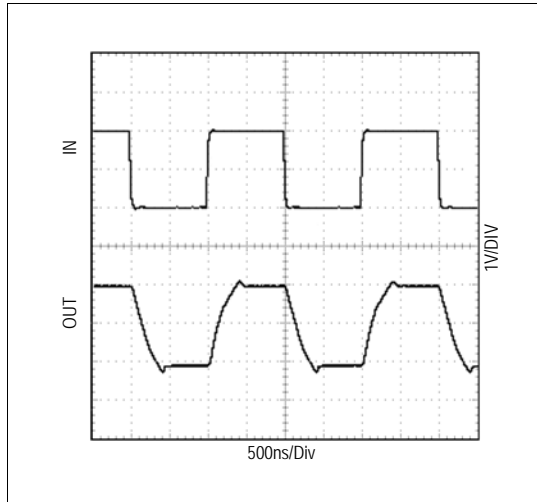
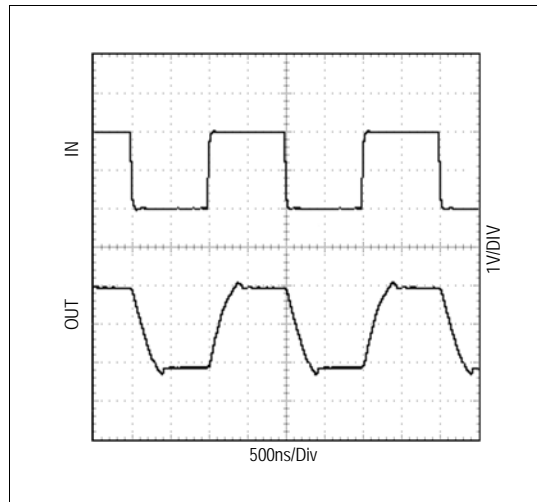


Figure 20. Transient Response, 2V, 100pF load



## 8 Application Information

### 8.1 Package Power Dissipation

**Caution:** Due to the high output current drive, this op-amp can exceed the absolute maximum power-dissipation rating. Normally, when peak current is less than or equal to 40mA the maximum package power dissipation is not exceeded for any of the package types offered.

The absolute maximum power-dissipation rating of each package should always be verified. (EQ 1) gives an approximation of the package power dissipation:

$$P_{\text{PACKAGEDISS}} \cong V_{\text{RMS}} I_{\text{RMS}} \cos\theta \quad (\text{EQ 1})$$

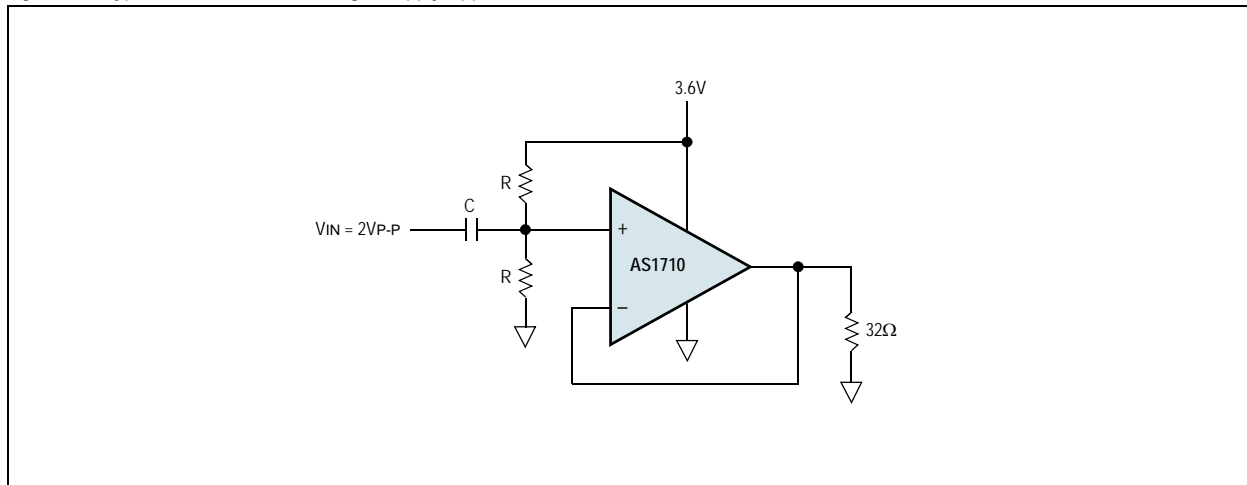
**Where:**

$V_{\text{RMS}}$  is the RMS voltage from  $V_{\text{DD}}$  to  $V_{\text{OUT}}$  when sourcing current, and from  $V_{\text{OUT}}$  to  $V_{\text{SS}}$  when sinking current.

$I_{\text{RMS}}$  is the RMS current flowing in or out of the op-amp and the load.

$\theta$  is the phase difference between the voltage and the current. For resistive loads,  $\cos\theta = 1$ .

Figure 21. Typical AS1710/AS1712 Single-Supply Application



$V_{\text{RMS}}$  can be calculated as:

$$V_{\text{RMS}} \cong (V_{\text{DD}} - V_{\text{DC}}) + V_{\text{PEAK}} / \sqrt{2} \quad (\text{EQ 2})$$

**Where:**

$V_{\text{DC}}$  is the DC component of the output voltage.

$V_{\text{PEAK}}$  is the highest positive excursion of the AC component of the output voltage.

For the circuit shown in Figure 21:

$$V_{\text{RMS}} = (3.6\text{V} - 1.8\text{V}) + 1.0\text{V} / \sqrt{2} = 2.507\text{VRMS}$$

$I_{\text{RMS}}$  can be calculated as:

$$I_{\text{RMS}} \cong I_{\text{DC}} + (I_{\text{PEAK}} / \sqrt{2}) \quad (\text{EQ 3})$$

**Where:**

$I_{\text{DC}}$  is the DC component of the output current.

$I_{\text{PEAK}}$  is the highest positive excursion of the AC component of the output current.

For the circuit shown in Figure 21:

$$I_{\text{RMS}} = (1.8\text{V} / 32\Omega) + (1.0\text{V} / 32\Omega) / \sqrt{2} = 78.4\text{mARMS}$$

Therefore, for the circuit in Figure 21 the package power dissipation can be calculated as:

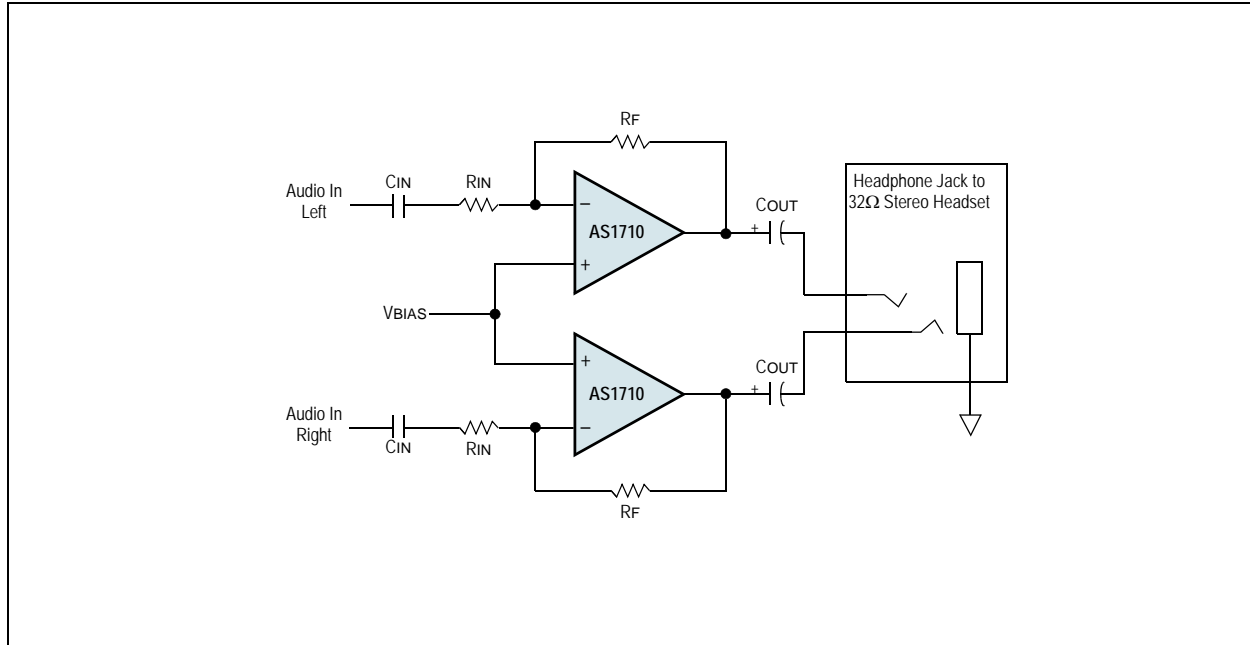
$$P_{\text{PACKAGEDISS}} = V_{\text{RMS}} I_{\text{RMS}} \cos\theta = 196\text{mW}$$

Adding a coupling capacitor improves the package power dissipation because there is no DC current to the load, as shown in Figure 22 on page 11.

## 8.2 60mW Single-Supply Stereo Headphone Driver

Two AS1710 amplifiers can be used as a single-supply, stereo headphone driver. The circuit shown in Figure 22 can deliver 60mW per channel with 1% distortion from a single 5V supply.

Figure 22. Stereo Headphone Driver Application (with Coupling Capacitor)



In Figure 22,  $C_{IN}$  and  $R_{IN}$  form a high-pass filter that removes the DC bias from the incoming signal. The -3dB point of the high-pass filter is given by:

$$f_{-3dB} = 1/(2\pi R_{IN}C_{IN}) \quad (EQ 4)$$

Choose gain-setting resistors  $R_{IN}$  and  $R_F$  according to the amount of desired gain, keeping in mind the maximum output amplitude.

$C_{OUT}$  blocks the DC component of the amplifier output, preventing DC current flowing to the load. The output capacitor and the load impedance form a high-pass filter with the -3dB point determined by:

$$f_{-3dB} = 1/(2\pi R_{LOAD}C_{OUT}) \quad (EQ 5)$$

For a 32Ω load, a 100μF aluminum electrolytic capacitor gives a low-frequency pole at 50Hz.

## 8.3 Rail-to-Rail Input Stage

The AS1710/AS1712 CMOS op-amps have parallel connected N- and P-channel differential input stages that combine to accept a common-mode range extending to both supply rails. The N-channel stage is active for common-mode input voltages typically greater than  $(V_{SS} + 1.2V)$ , and the p-channel stage is active for common-mode input voltages typically less than  $(V_{DD} - 1.2V)$ .

## 8.4 Rail-to-Rail Output Stage

The minimum output is within millivolts of ground for single-supply operation, where the load is referenced to ground ( $V_{SS}$ ). Figure 23 shows the input voltage range and the output voltage swing of an AS1710 connected as a voltage follower. The maximum output voltage swing is load dependent although it is guaranteed to be within 500mV of the positive rail ( $V_{DD} = 2.7V$ ) even with maximum load (32Ω to ground).

Figure 23. Rail-to-Rail Input/Output Range, 100kΩ

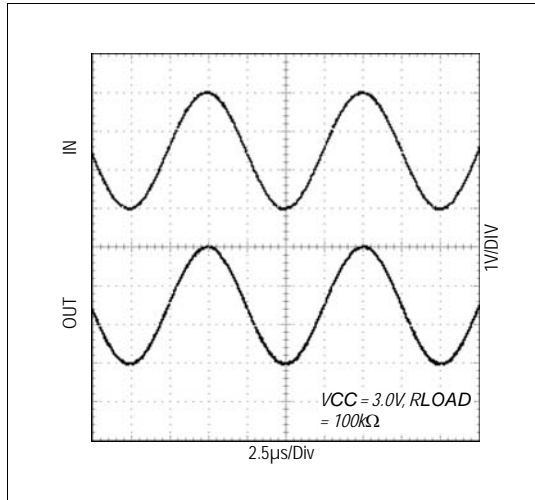
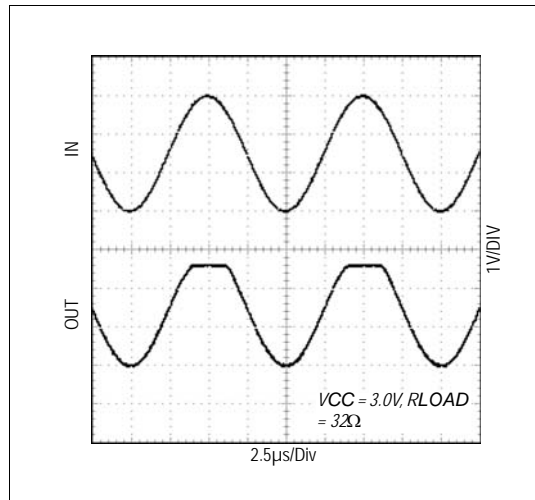


Figure 24. Rail-to-Rail Input/Output Range, 32Ω

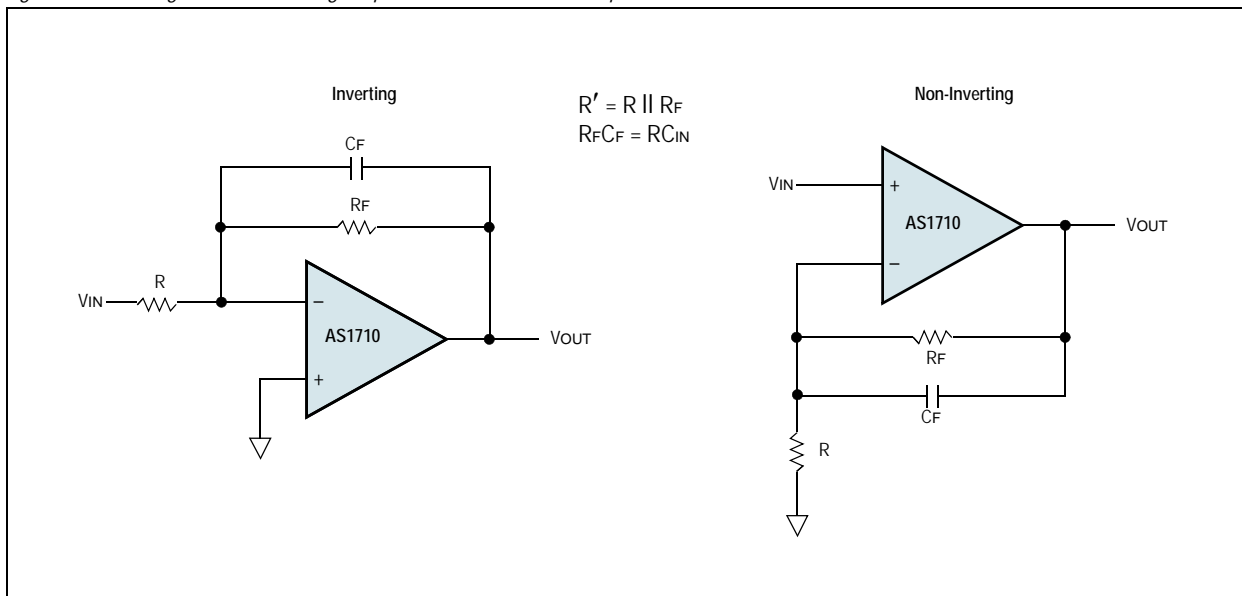


**Note:** The absolute maximum ratings (see page 3) for power dissipation and output short-circuit duration (10s, max) must be adhered to since the output current can exceed 200mA (see Typical Operating Characteristics on page 6).

## 8.5 Input Capacitance

The parallel-connected differential input stages for rail-to-rail operation results in relatively large input capacitance  $C_{IN}$  (6pF typ). This introduces a pole at frequency  $(2\pi R' C_{IN})^{-1}$ , where  $R'$  is the parallel combination of the gain-setting resistors for the inverting or non-inverting amplifier configuration (Figure 25). If the pole frequency is less than or comparable to the unity-gain bandwidth (10MHz), the phase margin is reduced, and the amplifier exhibits degraded AC performance through either ringing in the step response or sustained oscillations.

Figure 25. Inverting and Non-inverting Amplifiers with Feedback Compensation



The pole frequency is 10MHz when  $R' = 2k\Omega$ . To maximize stability,  $R' \ll 2k\Omega$  is recommended.

To improve step response when  $R' > 2k\Omega$ , connect a small capacitor ( $C_F$ ) between the inverting input and output.  $C_F$  can be calculated by:

$$C_F = 6(R/R_F) \text{ [pF]} \quad (\text{EQ 6})$$

### Where:

$R_F$  is the feedback resistor.

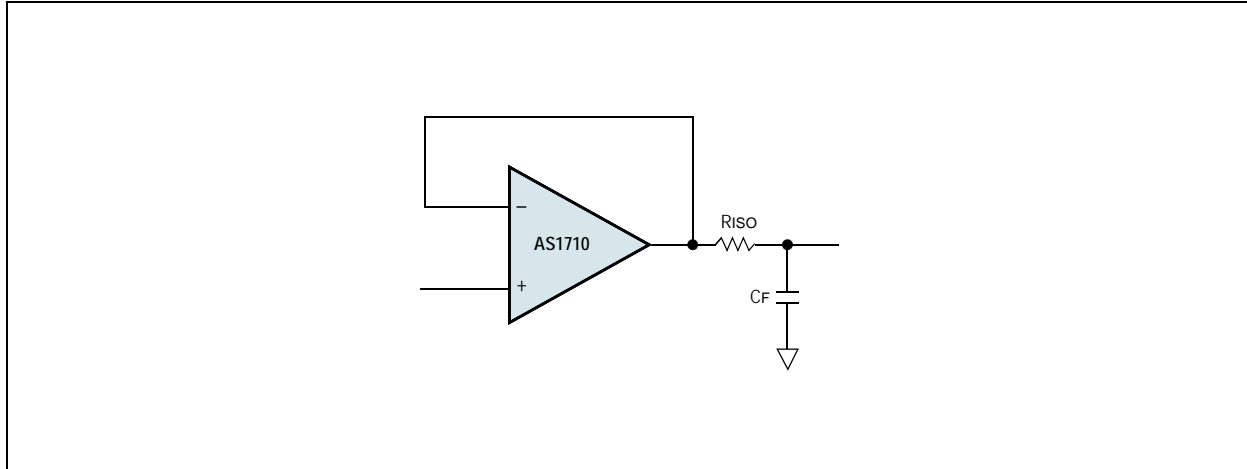
$R$  is the gain-setting resistor.

## 8.6 Driving Capacitive Loads

The AS1710/AS1712 amplifiers have a high tolerance for capacitive loads, and are stable with capacitive loads up to 100pF.

Figure 26 shows a typical non-inverting capacitive-load driving circuit in the unity-gain configuration.

Figure 26. Capacitive-Load Driving Circuit



**Note:** Resistor RISO improves the circuit's phase margin by isolating the load capacitor from the AS1710/AS1712 output.

## 8.7 Power-Up

The AS1710/AS1712 typically settle within 5 $\mu$ s after power-up.

## 8.8 Shutdown

When SHDNN (not included in B versions) is pulled low, supply current drops to 0.5 $\mu$ A (per amplifier,  $V_{DD} = 2.7V$ ), the amplifiers are disabled, and their outputs are driven to VSS. Because the outputs are actively driven to VSS in shutdown, any pull-up resistor on the output causes a current drain from the supply.

**Note:** Pulling SHDNN high enables the amplifier. In the AS1712 the amplifiers shutdown in pairs.

When exiting shutdown, there is a 6 $\mu$ s delay before the amplifier output becomes active.

## 8.9 Power Supplies and Layout

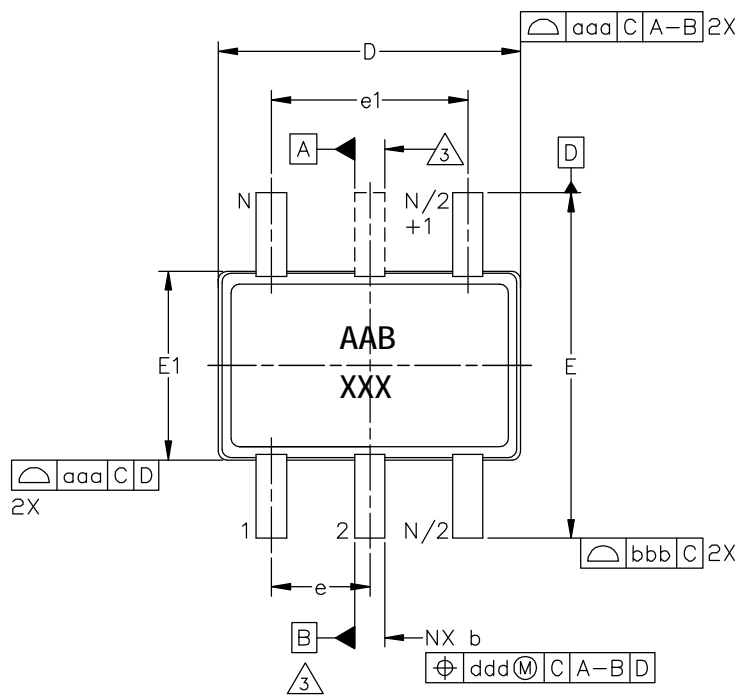
The AS1710/AS1712 can operate from a single 2.7 to 5.5V supply or from dual  $\pm 1.35$  to  $\pm 2.5V$  supplies. Good design improves device performance by decreasing the amount of stray capacitance at the op-amp inputs/outputs.

- For single-supply operation, bypass the power supply with a 0.1 $\mu$ F ceramic capacitor.
- For dual-supply operation, bypass each supply to ground.
- Decrease stray capacitance by placing external components close to the op-amp pins, minimizing trace and lead lengths.

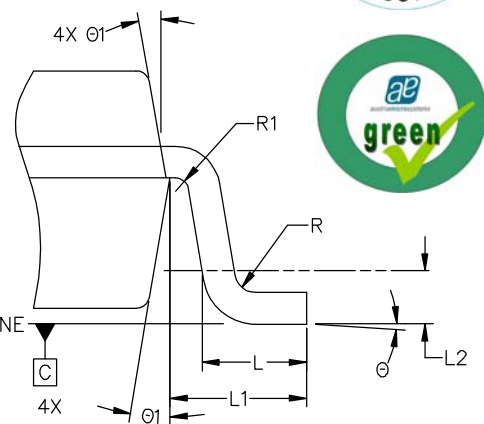
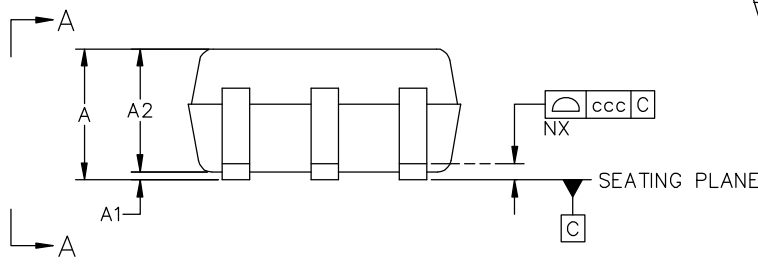
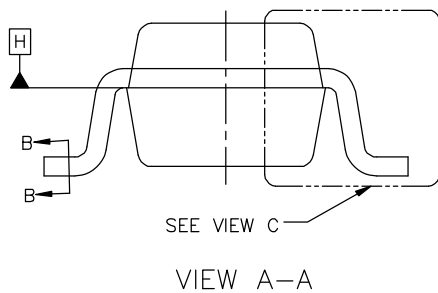
## 9 Package Drawings and Markings

The devices are available in a SC70-5, SC70-6, and TQFN-16 (3x3mm) package.

Figure 27. SC70-5 Package



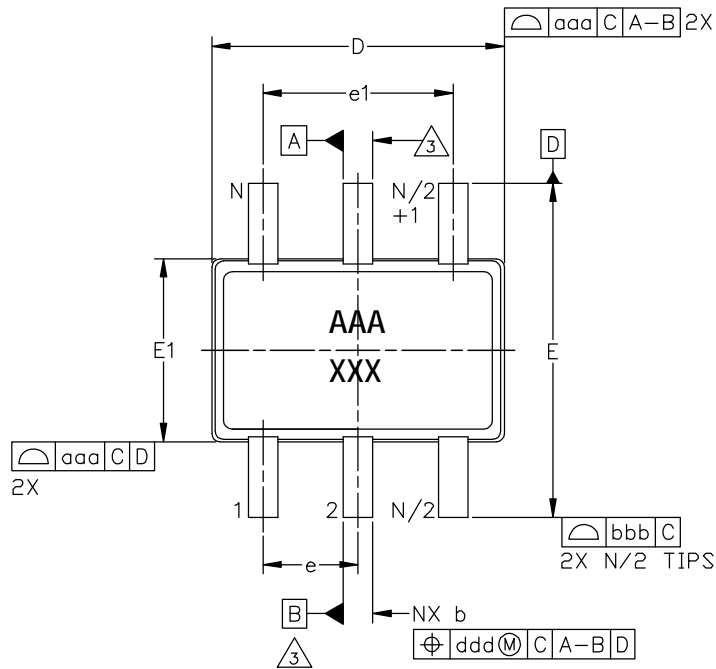
| Symbol     | Min      | Nom  | Max  |
|------------|----------|------|------|
| A          | -        | -    | 1.10 |
| A1         | -        | -    | 0.10 |
| A2         | 0.70     | 0.90 | 1.00 |
| b          | 0.15     | -    | 0.30 |
| c          | 0.08     | -    | 0.22 |
| D          | 2.00 BSC |      |      |
| E          | 2.10 BSC |      |      |
| E1         | 1.25 BSC |      |      |
| e          | 0.65 BSC |      |      |
| e1         | 1.30 BSC |      |      |
| L          | 0.26     | 0.36 | 0.46 |
| L1         | 0.42 REF |      |      |
| L2         | 0.15 BSC |      |      |
| R          | 0.10     | -    | -    |
| R1         | 0.10     | -    | 0.25 |
| $\theta$   | 0°       | 4°   | 8°   |
| $\theta_1$ | 4°       | -    | 12°  |
| aaa        | -        | 0.15 | -    |
| bbb        | -        | 0.30 | -    |
| ccc        | -        | 0.10 | -    |
| ddd        | -        | 0.10 | -    |
| N          | 5        |      |      |



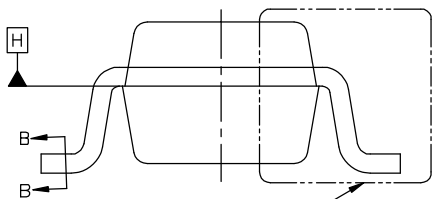
**Notes:**

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Datums A and B to be determined at datum H.

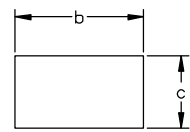
Figure 28. SC70-6 Package



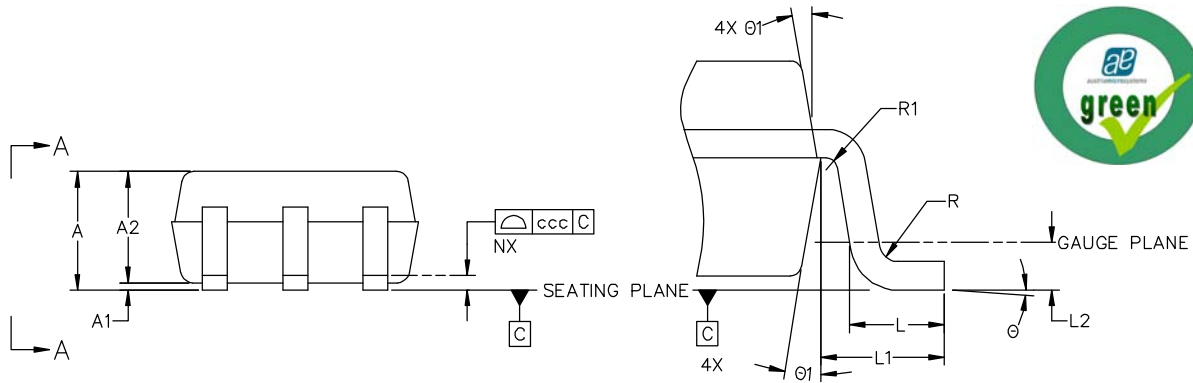
| Symbol     | Min      | Nom  | Max  |
|------------|----------|------|------|
| A          | -        | -    | 1.10 |
| A1         | -        | -    | 0.10 |
| A2         | 0.70     | 0.90 | 1.00 |
| b          | 0.15     | -    | 0.30 |
| c          | 0.08     | -    | 0.22 |
| D          | 2.00 BSC |      |      |
| E          | 2.10 BSC |      |      |
| E1         | 1.25 BSC |      |      |
| e          | 0.65 BSC |      |      |
| e1         | 1.30 BSC |      |      |
| L          | 0.26     | 0.36 | 0.46 |
| L1         | 0.42 REF |      |      |
| L2         | 0.15 BSC |      |      |
| R          | 0.10     | -    | -    |
| R1         | 0.10     | -    | 0.25 |
| $\theta$   | 0°       | 4°   | 8°   |
| $\theta_1$ | 4°       | -    | 12°  |
| aaa        | -        | 0.15 | -    |
| bbb        | -        | 0.30 | -    |
| ccc        | -        | 0.10 | -    |
| ddd        | -        | 0.10 | -    |
| N          | 6        |      |      |



SEE VIEW C  
VIEW A-A



SECTION B-B

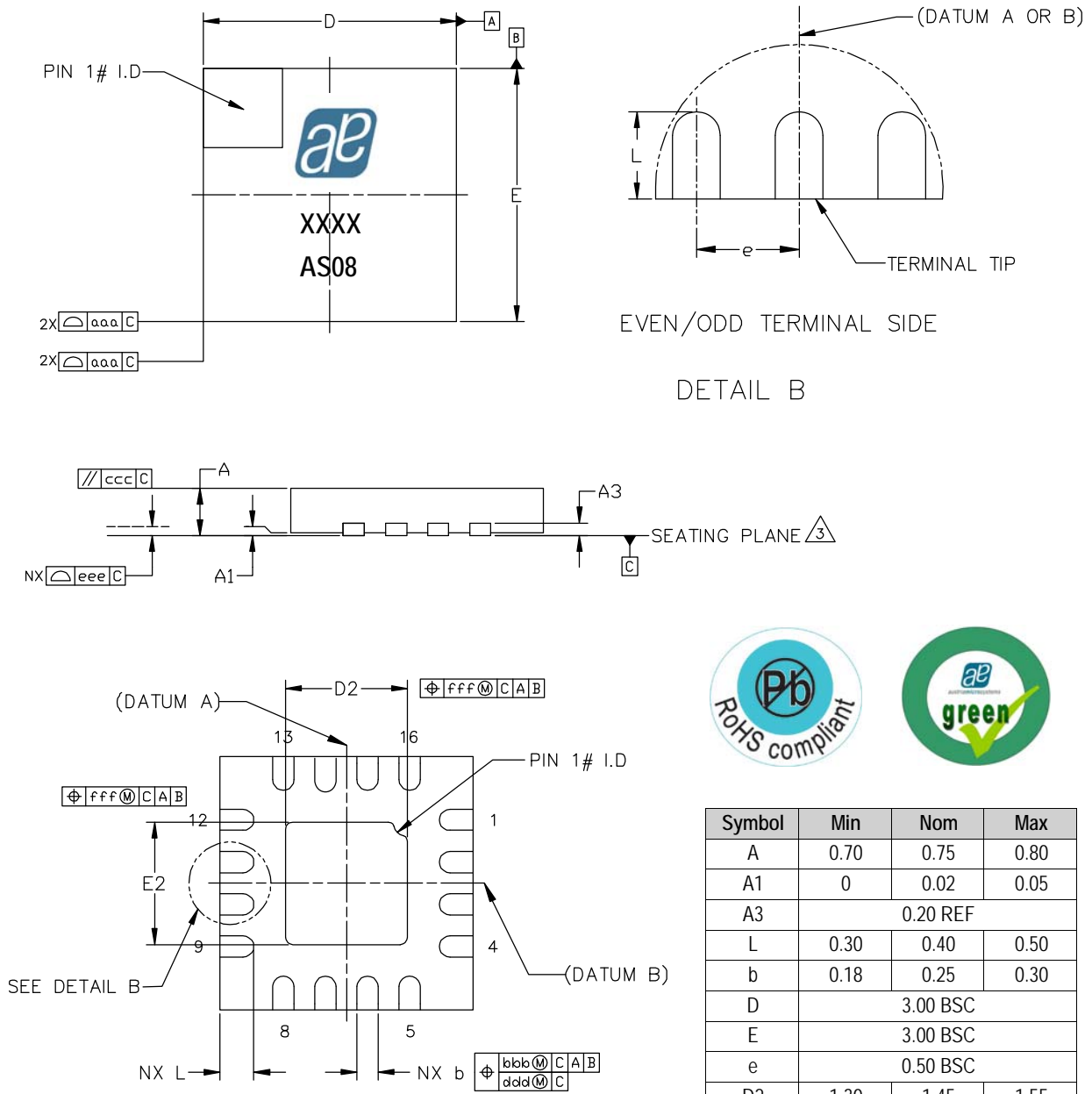


VIEW C

**Notes:**

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Datums A and B to be determined at datum H.

Figure 29. TQFN-16 (3x3mm)



| Symbol | Min      | Nom  | Max  |
|--------|----------|------|------|
| A      | 0.70     | 0.75 | 0.80 |
| A1     | 0        | 0.02 | 0.05 |
| A3     | 0.20 REF |      |      |
| L      | 0.30     | 0.40 | 0.50 |
| b      | 0.18     | 0.25 | 0.30 |
| D      | 3.00 BSC |      |      |
| E      | 3.00 BSC |      |      |
| e      | 0.50 BSC |      |      |
| D2     | 1.30     | 1.45 | 1.55 |
| E2     | 1.30     | 1.45 | 1.55 |
| aaa    | -        | 0.15 | -    |
| bbb    | -        | 0.10 | -    |
| ccc    | -        | 0.10 | -    |
| ddd    | -        | 0.05 | -    |
| eee    | -        | 0.08 | -    |
| fff    | -        | 0.10 | -    |
| N      | 16       |      |      |

**Notes:**

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

## Revision History

| Revision | Date         | Owner | Description   |
|----------|--------------|-------|---|
| 1.8      | -            | -     | Initial revision  |
| 1.9      | 01 Aug, 2011 | afe   | Updated <a href="#">Electrical Characteristics (page 4)</a> , <a href="#">Package Drawings and Markings (page 14)</a> . |

**Note:** Typos may not be explicitly mentioned under revision history.

## 10 Ordering Information

The device is available as the standard products shown in [Table 6](#).

*Table 6. Ordering Information*

| Ordering Code | Marking | Description                 | Delivery Form | Package         |
|---------------|---------|-----------------------------|---------------|-----------------|
| AS1710A-ASCT  | AAA     | Single Op Amp with Shutdown | Tape and Reel | SC70-6          |
| AS1710B-ASCT  | AAB     | Single Op Amp               | Tape and Reel | SC70-5          |
| AS1712A-AQFT  | ASO8    | Quad Op Amp with Shutdown   | Tape and Reel | TOFN-16 (3x3mm) |

**Note:** All products are RoHS compliant and austriamicrosystems green.  
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or find your local distributor at <http://www.austriamicrosystems.com/distributor>

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